NCERT SOLUTIONS
CLASS-XII PHYSICS
CHAPTER-14
SEMICONDUCTOR DEVICES

Q 1. Find which of the given statement is true for an n – type silicon.

(a) Majority carriers are the electrons and dopants are the trivalent.

(b) Minority carriers are the electrons and dopants are the pentavalents.

(c) Minority carriers are the holes and dopants are the pentavalent.

(d) Majority carriers are the holes and dopants are the trivalent.

Ans:

Here, (c) is the correct statement.

If we will take the case of n – type silicon, then the electrons will be the majority carriers, while the holes will be the minority carriers. We can obtain n – type semiconductor by dropping pentavalent atoms, such as phosphorus in silicon atoms.

Q2. Find the correct statement in the pervious question for a p – type semiconductors.

Ans:

Here, (d) is the correct statement.

In a p- type semiconductors the majority carriers are the holes, while the electrons works as the minority carriers. We can obtain a p – type semiconductor by dropping a trivalent atoms, such as aluminum, in silicon atoms.

Q 3. We have Silicon, carbon and germanium, each of them are having four valence electrons. Here, there are categorized by their conduction and valence band which are separated by energy gap respectively equal to $(E_g)_{Si}$, $(E_g)_c$ and $(E_g)_{Ge}$. Find out the correct statement.

(a) $(E_g)_{Si} < (E_g)_{Ge} < (E_g)_C$

(b) $(E_g)_C < (E_g)_{Ge} < (E_g)_{Si}$

(c) $(E_g)_C < (E_g)_{Si} < (E_g)_{Ge}$

(d) $(E_g)_C < (E_g)_{Si} < (E_g)_{Ge}$

Ans:

(C) is the correct statement.

Among the given three elements, Carbon has the maximum energy gap while germanium u=is having the least energy band gap.

The energy band gap of these elements is related as : $(E_g)_C < (E_g)_{Si} < (E_g)_{Ge}$

Q 4. In an unbiased p – n junction, holes diffuses to n – region from p – region because

(a) The electron in the n – region and which of them are free attracts them

(b) They are moved to the junction by the potential difference.

(c) The concentration of the holes at p – region is more as compared to that of the n – region

(d) All of the above.

Ans:

(c) is the correct statement.

The charge carriers diffuse across a junction as it moves from the higher concentration region to the lower concentration region. Here in the above case, greater concentrations of holes are at the p – region as compared to the n – region. Hence, in an unbiased p – n junction, holes diffuses from the p – region to the n – region.

Q 5. When a p – n junction is forward biased, its

(a) potential power is increased.

(b) majority carrier current is reduced to zero.

(c) potential barrier is reduced.

(d) None of the above.

Ans:

(c) is the correct statement

When we will apply the forward bias to a p – n junction, its potential barrier is reduced.

In the above condition of forward bias, the applied voltage is opposed by the potential barrier. Hence, the potential barrier across the junction gets reduced.

Q 6. Find out the correct statements from the following for the case of a transistor action

(a)Emitter, collector and base regions should have same size and doping concentration

(b) The base region must be very thin and lightly doped.

(c) The collector junction is reverse biased and the emitter unction is forward biased.

(d) Both of the emitter and the collector junction are forward biased.

Ans:

(b) and (c) are the correct statements.

In the case of a transistor action,for the base region to be very thin the junction must be lightly doped. Also, the collector junction needs to be reverse – biased and the emitter junction needs to be forward biased

Q 7. In the case of a transistor amplifier, the voltage gain

(a) Does not change for any frequencies.

(b) Will remain constant in the middle frequency and it will be high at high and low frequency.

(c) Will remain constant at middle frequency and it will be low at high and low frequencies.

(d) None of the above.

Ans:

(c) is the correct statement.

The voltage gain of a transistor amplifier will remain constant at middle frequency and it will be low at high and low frequencies.

Q 8. Calculate the output frequency of a half – wave rectifier, if we will provide an input with frequency 50 Hz. Also calculate the output frequency for a full wave rectifier if the input is given the same.

Ans:

Input frequency = 50 Hz.

In the case of a half – wave rectifier the output frequency will remain the same as the input frequency.

Therefore, **Output frequency = 50 Hz**

Therefore, **Output frequency = 50 Hz.**

While in the case of full – wave rectifier the output frequency gets double the input frequency.

Therefore, **Output frequency = 2 × 50 = 100 Hz**

Q 9 . Find the input signal voltage and base current for a CE – transistor amplifier, the voltage of audio signal across the collector resistance of $2k\Omega$ is 2 V. Assume that the transistor have current amplification factor equals to 100 and the given base resistance is $1k\Omega$

Ans:

Collector resistance, $R_C = 2k\Omega = 2000\Omega$

Voltage of audio signal across the collector resistance, V = 2V

Current amplification factor of the transistor, $\beta = 100$

Base resistance, $R_B = 1k\Omega = 1000\Omega$

Input Signal = V_i

Base current = I_B

We have amplification relation as:

$\frac{V}{V_i} = \beta \frac{R_C}{R_B}$

Voltage amplification

$V_i = \frac{V}{\beta} \frac{R_B}{R_C} = \frac{2\times}{100\times} \frac{1000}{2000} = 0.01V$

Therefore, the input signal voltage of the amplifier is 0.01 V.

Base resistance is given by the relation:

$R_B = \frac{V_i}{I_B}$
$= \frac{0.01}{1000} = 10^{-6} \times 10\mu A$

Therefore, the base current of the amplifier is 10 A.

Q 10. Calculate the output ac signal, if two amplifiers are connected in series one after another (cascaded). Where the voltage gain for first amplifier is 20 and for the second it is 40. And the input signal is provided for 0.01 volt, calculate the output ac signal.

Ans:

For 1st amplifier, Voltage gain, $V_1 = 20$

For 2nd amplifier, Voltage gain, $V_2 = 40$

Input signal voltage, $V_i = 0.01\ V$

Output AC signal voltage = V_O

Thus, we can calculate the total voltage gain for the two – stage cascaded amplifier by multiplying the voltage gains for each of the individual stages, i.e.,

$V = V_1 \times V_2$

= 20 × 40

= 800

We know that:

$V = \frac{V_o}{V_i}$
$V_o = V \times V_i$

= 800 × 0.01 = 8 V

Therefore, the output AC signal of the given amplifier is 8 V.

Q 11.Is it possible for a p – n photodiode to detect a wavelength of 5000 nm, if it is fabricated from a semiconductor with a band gap of 3.2 eV?

Ans:

Energy band gap for the photodiode = $E_g = 3.2\,eV$

Wavelength, λ = 5000 nm = $5000 \times 10^{-9} m$

We know from the relation of energy:

$E = \frac{hc}{\lambda}$

Where, h = Planck's constant = $6.626 \times 10^{-34}\,Js$

C = Speed of light

=$3 \times 10^8\,m/sec$

$\therefore E = \frac{6.626 \times 10^{-34} \times 3 \times 10^8}{5000 \times 10^{-9}}$

$3.975 \times 10^{-20} J$

But $1.6 \times 10^{-19} J = 1\ eV$

$\therefore E = 3.975 \times 10^{-20} j$

$= \frac{3.975 \times 10^{-20}}{1.6 \times 10^{-19}} = 0.248\ eV$

Thus, we get the energy of a signal of wavelength 5000 nm is 0.248 eV, which is less than 3.2 eV, the energy band gap of a photodiode. Hence, the photodiode cannot detect the signal.

Additional Exercises

Q 12. We have $5 \times 10^{28}\ per\ m^3$ silicon atoms with us. Which is doped with $5 \times 10^{22}\ per\ m^3$ of Indium and $5 \times 10^{20}\ per\ m^3$ of Arsenic simultaneously. Find out the total number of holes and the electrons. We are given,$n_i = 1.5 \times 10^{16}\,m^{-3}$. Also find if the material n – type or p – type?

Ans:

Number of Atoms (Silicon), N = $5 \times 10^{28}\ atoms/m^3$

Number of Atoms (Arsenic), $n_{As} = 5 \times 10^{28}\ atoms/m^3$

Number of Atoms (indium), $n_{In} = 5 \times 10^{20}\ atoms/m^3$

Number of thermally generated electrons, $n_i = 1.5 \times 10^{16}\ electrons/m^3$

Number of electrons, $n_e = 5 \times 10^{22} - 1.5 \times 10^{16} \approx 4.99 \times 10^{22}$

Number of holes = n_h

In the case of thermal equilibrium, the concentration of electrons and holes in a semiconductor are related as: $n_e n_h = n_i^2$

$\therefore n_h = \frac{n_i^2}{n_e}$

$= \frac{(1.5 \times 10^{16})^2}{4.99 \times 10^{22}} \approx 4.51 \times 10^9$

Therefore, there are approximately 4.99×10^{22} and holes are around 4.51×10^9. Since the number of electrons here is more than that of the holes. So, the material we have is an n – type semiconductor.

Q 13. Calculate the ratio between conductivity at 600 k and that at 300 k when an intrinsic semiconductor having energy gap E_g eV. Whose whole is much smaller than electron mobility and independent of temperature. Assume that the temperature dependence of intrinsic carrier concentration is given by

$n_i = n_0\, exp\left[-\frac{E_g}{2k_B T}\right]$

Where n_0 is a constant.

Ans: Energy gap of the given intrinsic semiconductor, $E_g = 1.2\ eV$

We can write the temperature dependence intrinsic carrier – concentration:

$n_i = n_0\, exp\left[-\frac{E_g}{2K_BT}\right]$

Where k_B = Boltzmann constant = $8.62 \times 10^{-5} eV/K$

T = temperature

n_0 = Constant

Initial temperature, T_1 = 300 K

We can write the intrinsic – concentration at this temperature as:

$n_{i1} = n_0\, exp\left[-\frac{E_g}{2K_B \times 300}\right] \ldots (1)$

Final temperature, T_2 = 600 K

We can write the intrinsic – concentration at this temperature as:

$n_{i2} = n_0\, exp\left[-\frac{E_g}{2K_B \times 600}\right] \ldots (2)$

The ratio between the conductivities at 600 K and at 300 K is equal to the ratio between the respective intrinsic carrier-concentrations at these temperatures.

$$\frac{n_{i2}}{n_{i1}} = \frac{n_0\, exp\left[-\frac{E_g}{2K_B \times 600}\right]}{n_0\, exp\left[-\frac{E_g}{2K_B \times 300}\right]} = exp\, \frac{E_g}{2k_B}\left[\frac{1}{300} - \frac{1}{600}\right]$$
$$= exp\left[\frac{1.2}{2 \times 8.62 \times 10^{-5}} \times \frac{2-1}{600}\right]$$
$$= exp\,[11.6] = 1.09 \times 10^5$$

Therefore, the ratio between the conductivities is 1.09×10^5.

Q 14. The current I for a p – n junction diode can be expressed as:

$I = I_0\, exp\left(\frac{eV}{2K_BT} - 1\right)$

Where I_0 is called the reverse saturation current, v is the voltage across the diode and is positive for forward bias and negative for reverse bias, and I is the current through the diode, k_B is the Boltzmann constant ($8.62 \times 10^{-5} eV/K$) and T is the absolute temperature. It is for a given diode $I_0 = 5 \times 10^{-12}$ A and t = 300 K, then

(a) What will be the forward current at a forward voltage of 0.6 V?

(b) What will be the increase in the current if the voltage across the diode is increasedto 0.7 V?

(c) What is the dynamic resistance?

(d) What will be the current if reverse bias voltage changes from 1 V to 2 V?

Ans:

In a p-n junction diode, the expression for current is given as:

$I = I_0\, exp\left(\frac{eV}{2K_BT} - 1\right)$

I_0 = Reverse saturation current =5×10^{-12}

k_B = Boltzmann constant = $8.62 \times 10^{-5} eV/K$ = $1.376 \times 10^{-23} JK^{-1}$

V = Voltage across the diode.

(a) Forward voltage, V = 0.6 V

$$\therefore Current\ I = 5 \times 10^{-12}\left[exp\left(\frac{1.6 \times 10^{-19} \times 0.6}{1.376 \times 10^{-23} \times 300}\right) - 1\right]$$
$$= 5 \times 10^{-12} \times esp\,[22.36] = 0.0256\ A$$

Therefore, the forward current is about 0.0256 A.

(b) For forward voltage, V = 0.7 V, we can write:

$$I^{'} = 5 \times 10^{-12}\left[exp\left(\frac{1.6 \times 10^{-19} \times 0.7}{1.376 \times 10^{-23} \times 300} - 1\right)\right]$$
$$= 5 \times 10^{-12} \times exp\,[26.25] = 1.257\ A$$

Hence, the increase in current, $\Delta I = I^{'} - I$

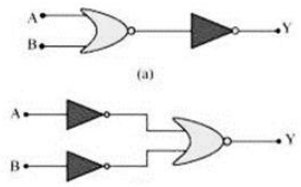
= 1.257 – 0.0256 = 1.23 A

(c) Dynamic Resistance = $\frac{Change\ in\ voltage}{Change\ in\ current}$

$= \frac{0.7-0.6}{1.23} = \frac{0.1}{1.23} = 0.081\Omega$

(d) If the reverse bias voltage changes from 1 V to 2 V, then the current (I) will almost remain equal to I_0 in both cases. Therefore, the dynamic resistance in the reverse bias will be infinite.

Q 15. From the provided two circuits, show that circuit (a) and circuit (b) acts as OR gate and AND gate respectively.



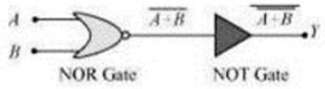
Ans:

(a) Input for the circuit : A and B

Output for the circuit: Y

Here, the left half of the circuits works as the NOR gate, while if we look at the right half of the circuit then it is a NOT gate.

We can show it in figure as:



Now, the output for the NOR gate = $\overline{A+B}$

We are giving the output from NOR gate to the input at NOT gate.So, its output will be:$\overline{\overline{A+B}}$ = A + B

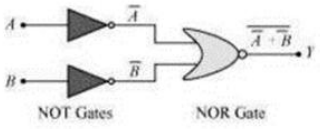
$\therefore Y = A + B$

Hence, this circuit functions as an OR Gate.

(b) Input for the circuit : A and B

Output for the circuit: Y

We can observe from the figure that the output from first half of the circuits goes to the input of the next half which is working as NOR gate.

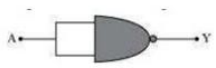


Hence, the output of the given circuit can be written as:

$Y = \overline{\bar{A}+\bar{B}} = \bar{\bar{A}}.\bar{\bar{B}} = A.B$

Hence, this circuit functions as an AND gate.

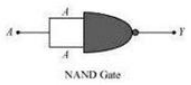
Q 16. Write the truth table for a NAND gate connected as shown in the figure.



And then find out the exact login operation carried out by the given circuit.

Ans:

From the figure, we know A is the input and we are getting an output B.



Hence, the output can be written as:

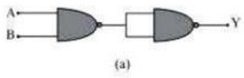
$$Y = \overline{A.A} = \bar{A} + \bar{A} = \bar{A}$$

We can make the truth table for eq(1) as:

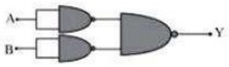
A	Y
0	1
1	0

So, this circuit works as a NOT gate. The symbol for this this circuit is shown as:

Q 17. You have two circuits consisting NAND gates arranged to perform different logical operations. Identify the logical operation carried by the two circuits (Shown in figure).



(a)

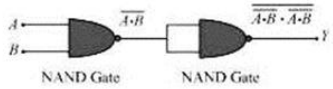


(b)

Ans:

In both the circuits, A and B are the inputs and Y is the output.

(a) The output of the left NAND gate will be $\overline{A.B}$, as shown in the following figure.

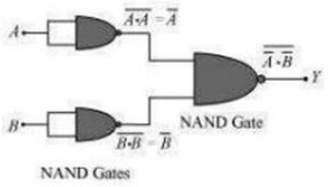


Hence, the output for these two NAND gate is given as:

$$Y = \overline{\left(\overline{A.B}\right).\left(\overline{A.B}\right)} = \overline{\overline{AB}} + \overline{\overline{AB}} = AB$$

Therefore, this circuit works as an NAND gate.

(b) $\bar{A}$ is the output of the upper left of the NAND gate and $\bar{B}$ is the output of the lower half of the NAND gate, as shown in the following figure.



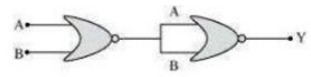
Hence, the output from this combination of NAND gates can be shown as:

$$Y = \bar{A}.\bar{B} = \bar{\bar{A}} + \bar{\bar{B}} = A + B$$

Therefore, we can say that this circuit is working as an OR gate.

Q 18. Draw the truth table for the circuit having NOR gates and find out the logic operation (OR, AND, NOT) which is formed by this circuit.

(Hint: A = 0, B = 1 then A and B inputs of second NOR gate will be 0 and hence Y=1. Similarly work out the values of Y for other combinations of A and B. Compare with thetruth table of OR, AND, NOT gates and find the correct one.)

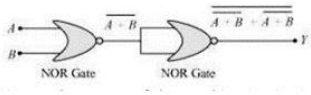


Ans

Input for the circuit: A and B

Output from the first circuit (i.e NOR gate) is $\overline{A+B}$.

From the figure we can observe that the input for the second gate is automatically the output from that first one.



Therefore, the output obtained from this combination is given as:

$$Y = \overline{\overline{A+B}+\overline{A+B}} = \overline{\bar{A}.\bar{B}} + \overline{\bar{A}.\bar{B}}$$
$$= \overline{\bar{A}.\bar{B}} = \bar{\bar{A}} + \bar{\bar{B}} = A + B$$

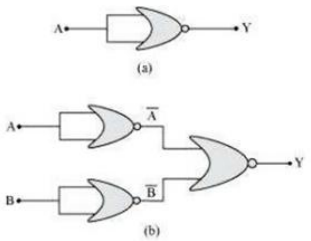
The truth table for this operation is given as:

A	B	Y (= A + B)
0	0	0
0	1	1
1	0	1
1	1	1

This is the truth table of an OR gate.

Therefore, this circuit functions as an OR gate.

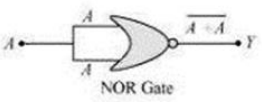
Q 19. Find out the truth table forming by combining the OR gates only. (as shown in the following figure). Identify the logic operation (OR, AND, NOT) performed by the two circuits



Ans:

(a) Here, A is acting as both the outputs for the NOR gate and Y is the output, as shown in the following figure.

So, the output of the circuit is $\overline{A+A}$.



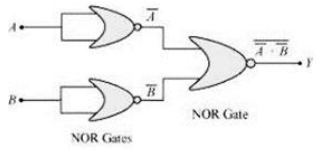
Output, Y = $\overline{A+A} = \bar{A}$

The truth table for the circuit is given as:

A	Y($\bar{A}$)
0	1
1	0

Here, we obtain the truth table for a NOT gate. Hence, the circuits works as a NOT gate.

(b) A and B are the inputs and Y is the output of the given circuit. By using the result obtained in solution (a), we can infer that the outputs of the first two NOR gates are $\bar{A}$ and $\bar{B}$, as shown in the figure.



$\bar{A}$ and $\bar{B}$ are the inputs for the last NOR gate. Hence, the output for the circuit can be written as:

A	B	Y (= A! B)
0	0	0
0	1	0
1	0	0
1	1	1

Here what we obtained is a truth table of an AND gate. Therefore, the circuit functions as an AND gate.